Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1 1-19. (Canceled) (New) A microprocessor-based system, comprising: 1 2 a microprocessor; 3 at least one peripheral device coupled to the microprocessor via a bus; 4 an address map coupled to the microprocessor, the address map storing address 5 allocated to the peripheral device to enable accesses thereto over said bus; 6 a peripheral control register coupled to receive peripheral control data from the 7 microprocessor; 8 peripheral device disable logic coupled between the peripheral control register 9 and to the peripheral device; and 10 address mapping logic coupled to the address map to automatically remove an 11 address space allocated to a disabled peripheral device from the address map, whereby an 12 address for the disabled peripheral device is not generated on the bus. 1 21. (New) The microprocessor-based system as claimed in claim 20, wherein 2 a peripheral device may be disabled by sending a logic signal from the peripheral control register 3 to the peripheral device disable logic associated with said peripheral device. 1 22. (New) The microprocessor-based system as claimed in claim 21, wherein, 2 when said logic signal is sent from the peripheral control register to the peripheral device disable 3 logic associated with said peripheral device, a corresponding logic signal is also sent to said address mapping logic to remove the address space for said disabled peripheral device from the 4 5 address map.

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- 1 23. (New) The microprocessor-based system as claimed in claim 20, having a 2 programmable address map, wherein, when the address space for said disabled peripheral device 3 is removed from the address map, a clock signal is automatically gated off from the peripheral 4 device.
 - 24. (New) The microprocessor-based system as claimed in claim 20, having a programmable address map, wherein, when the address space for said disabled peripheral device is removed from the address map, a logic signal is sent to said peripheral device disable logic to gate off the clock signal from the peripheral device, and thereby disable the peripheral device.
- 1 25. (New) The microprocessor-based system as claimed in claim 20, further 2 comprising a clock generator configured to supply a clock signal to each peripheral device, 3 through the associated peripheral device disable logic.
- 1 26. (New) The microprocessor-based system as claimed in claim 20, wherein 2 the system is implemented in an integrated circuit, and wherein at least one peripheral device 3 comprises an interface for an external device.
 - 27. (New) A microprocessor-based system as claimed in claim 20, wherein the system is implemented in a programmable logic integrated circuit, and wherein the microprocessor is provided as an embedded circuit, while at least one of the peripheral device is implemented in programmable logic.

L	28. (New) An integrated circuit, comprising.
2	a microprocessor coupled to a peripheral device via a bus;
3	address mapping logic coupled to an address map for storing addresses allocated
1	to peripheral device to enable accesses thereto over said bus; and
5	a peripheral control register coupled to receive peripheral control data form the
5	microprocessor, and configured to disable a peripheral device, and
7	wherein, when a peripheral device is disabled, said address allocated to the
3	disabled peripheral device is automatically removed from the address map to prevent further
)	access attempts thereto.
1	29. (New) The integrated circuit as claimed in claim 28, wherein said
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2	peripheral device comprises an interface to an external device.
l	30. (New) The integrated circuit as claimed in claim 28, wherein said
2	peripheral device is implemented in programmable logic.
1	31. (New) The integrated circuit as claimed in claim 28, wherein a peripheral
•	device may be disabled by sending a logic signal from the peripheral control register to the
- }	peripheral device disable logic associated with said peripheral device.
,	peripheral device disable legic associated with said peripheral device.
l	32. (New) The integrated circuit as claimed in claim 31, wherein, when said
2	logic signal is sent from the peripheral control register to the peripheral device disable logic
3	associated with said peripheral device, a corresponding logic signal is also sent to address
1	mapping logic to remove the address for said peripheral device from the address map.
l	33. (New) The integrated circuit as claimed in claim 31, further comprising a
)	clock generator configured to supply a clock signal to the peripheral device, through the
-	associated peripheral device disable logic.
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l	34. (New) The integrated circuit as claimed in claim 28, wherein said address
2	map is programmable, and wherein, when the address for a peripheral device is removed by said
3	microprocessor from the address map, a clock signal is prevented from reaching said peripheral
1	device to disable said peripheral devic.
l	35. (New) In a microprocessor-based system, comprising a microprocessor
2	coupled via a bus to at least one peripheral device, a method of operating the system comprising:
3	storing in an address map at least one address corresponding to the at least one
4	peripheral device;
5	disabling the at least on peripheral device; and
5	automatically removing from the address map an address corresponding to the
7	disabled peripheral device, thereby preventing further access attempts thereto via the bus.
l	36. (New) The method as claimed in claim 35, wherein disabling the at least
2	one peripheral device comprises supplying a first logic signal from a peripheral control register
3	to a peripheral device disable logic associated with said peripheral device.
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l	37. (New) The method as claimed in claim 35 wherein the disabling step
2	further comprises automatically gating off a clock signal from the peripheral device.
1	38. (New) The method as claimed in claim 36, wherein the step of
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2	automatically removing comprises supplying a second logic signal corresponding to the first
3	logic signal, to said address map to remove the address corresponding to the disabled peripheral
4	device from the address map.